An Analysis of D-Fuzzy Flip-Flop Design

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Abstract— **The paper presents the concept of existing D fuzzy flip-flop design and analyses the working of the design. The existing design has been studied for its delay parameters and variability. Comparisons with the previous designs has been done to lay down the superiority of the fuzzy design over existing binary flip-flop designs.**

Keywords— **Binary flip-flop, Fuzzy flip-flop, D fuzzy flip-flop, delay, variability.**

I.   INTRODUCTION

The change in the trend of the digital designing has motivated the flip-flop designing using fuzzy as a mathematical tool. The paper discusses the previous fuzzy flip-flop designs and focusses on the analysis of Modified D fuzzy flip-flop design. It has further shown the novelty of the design while discussing its delay values and calculated the variability of the design. Part II of the paper deals in the introduction to the previous designs of fuzzy flip-flops, part III states the concept of the flip-flop design and part IV analyses the working of the design while discussing the superiority of the design and part V concludes the paper.

II.   LITERATURE SURVEY

K. Hirota and K. Ozawa stated the concept of the JK fuzzy flip-flop circuit by providing the hardware implementation of the design. The design was found to have undesirable heating effects [1]. K. Ozawa and K. Hirota presented another type of fuzzy flip-flop called algebraic fuzzy flip-flop and found that the discrete mode design were more power effective in comparison to analog designs [2].

J. Diamond focused on the CMOS implementation of the JK flip-flop circuit and highlighted the usage of lukasciewicz connectives to design various fuzzy circuits [3].

L. Gniewek and J. Kluska improvised the new design of fuzzy flip-flops based on the bounded sum, product and complementation operations. It had introduced various models and discussed the relationship between these models in reference to the preservation of the binary flip-flop analogy [4].

B. Choi and K. Tipnis highlighted the need of fuzzy components to implement the fuzzy systems. The previous models of JK flip-flops evolved the existence of unstable states when implemented and these states remained unavoidable. The concept of D-fuzzy flip flop was targeted to remove the unstable states of the existing JK flip-flop models [5].

S. Chakraborty introduced way to overcome the unstable states of JK flip-flops stated earlier. It laid down the scope to remove the unresolved unstable states in the future [6].

B. Choi eliminated the unstable JK flip-flop states by introducing the D flip-flop design [7].

Himanshu et al. presented the analysis of existing D flip-flop designs in terms of delay, variability and robustness [8].

III.   CONCEPT OF THE D FUZZY FLIP-FLOP

The concept of D fuzzy flip-flop stated by B. Choi involved the min, max and complementation gates to design the D fuzzy flip-flop circuit. The D fuzzy flip-flop so introduced was free from the undesirable or unstable states as the flip-flop accepts a continuous signal and presents it at output after delay in the way similar to the binary flip-flops where each bit appears at output after some delay. The equation hereby shows the usage of fundamental fuzzy min and max gates to implement the existing design.

$$Q(t+1)=\min\{\{D\}, \{\max\{D, Q(t)\}, \max\{(1-Q(t)), D\}\} \tag{1}$$

where D is the input signal, $Q(t)$ is the previous output fed back and $Q(t+1)$ is the current output. Min and max are fuzzy min and max functions respectively.

The continuous signal has been sampled and discrete values so obtained have been operated by min, max and complementation functions as shown in the equation.

The graphical representation of the sinusoidal input has been done by plotting magnitude of the signal on y axis with increasing time on x axis as under:
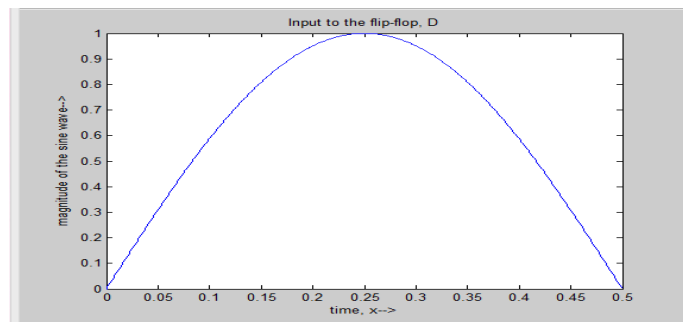

Fig 1 Magnitude Vs Time input signal characteristics of D fuzzy flip-flop.

Fig 1. has shown the continuous input signal characteristics in time range from 0 to 0.5 seconds. The input has been sampled and each sampled value has been operated with the fuzzy logic gates to realize the flip-flop. The input shown has ascending and descending positive values for given time range and the previous design was able to reproduce this input faithfully at output. Using equation (1), each sampled input has been operated by min, max and complementation operators to get the delayed output. The fig 2 has shown the output characteristics of the D fuzzy flip-flop. This design has neither taken clock as an input nor considered the negative values of the D input.
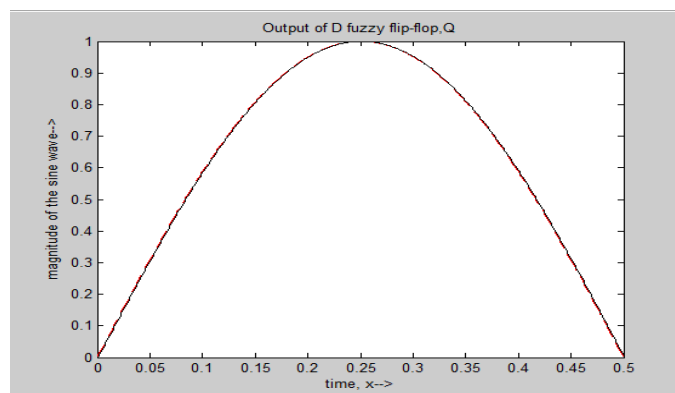

Fig 2 Magnitude Vs Time output characteristics of D fuzzy flip-flop.

The bold lines in the figure represents the output of the flip-flop. The output when compared with the input characteristics of the flip-flop design, both signals overlapped each other.

IV.   ANALYSIS OF THE D FUZZY FLIP-FLOP DESIGN

The results have been compiled in the terms of delay, variability and robustness. The calculated values have been compared with the existing values to show novelty of the work. The delay of the D Fuzzy Flip-Flop has been tabulated. The delay gives the magnitude of the delay to pass entire continuous signal (say sine wave) here to appear as output whereas the delay in binary flip-flops has defined the delay of one bit to appear at output. According to the tabulated delay for 10 simulations, standard deviation and variability of the design has been calculated. Table1 shows the calculated delay and summation of the delay in order to find the standard deviation and variability of the simulated design. The variability so calculated defines the variation in the results with respect to input and minimum variability ensures the higher robustness of the design. Robustness is the quality of the design when it has minimum sensitivity to the variability with respect to time, conditions and the environment [8]. The simulated design has been studied by repeating the simulation for number of times. The design has been thus studies for a different number of times to get the performance indices of the design in terms of variability.

The lower value of the variability signifies that the design is lesser prone to the changes in the output due to the presence of the variations in the input signal, changes in the propagation delay of the design. Thus, the design becomes efficient in terms of the variations shown in the working for the inputs provided to the design.

TABLE 1: THE TIME DELAY FOR CONTINUOUS SIGNAL INPUT TO D FUZZY FLIP-FLOP.

Sr. No.	Delay (x) in 10^{-5} seconds	(x-mean) in 10^{-6} seconds	(x-mean)^2 in 10^{-12} seconds
1.	2.3	0.7	0.49
2.	2.3	0.7	0.49
3.	2.4	1.7	2.89
4.	1.9	-3.3	10.89
5.	2.1	-1.3	1.69
6.	2.4	1.7	2.89
7.	1.9	-3.3	10.89
8.	2.1	-1.3	1.69
9.	2.1	-1.3	1.69
10.	2.3	0.7	0.49
$\sum_{i=1}^{n} X$	22.3		34.1

where,

$$mean = \frac{\sum_{i=1}^{10} x}{10} = \frac{22.3}{10} \times 10 - 5 = 2.23 \times 10 - 5 \; seconds$$

Standard Deviation has been calculated as per the equation:

$$\sqrt{\frac{\sum(x - mean)^2}{N}}$$

(2)

$$Standard \; Deviation = \sqrt{\frac{34.1}{10}} = 1.84 \times 10 - 6 \; seconds,$$

and,

$$Variability = \frac{Standard \; Deviation}{Mean}$$

(3)

Lesser the variability, higher is the robustness of the design. The variability has come out to be 0.0826 which is compared to the variability in existing designs. Later, it has been examined that the concept of fuzzy D flip-flop provides the higher robustness with respect to the existing designs.
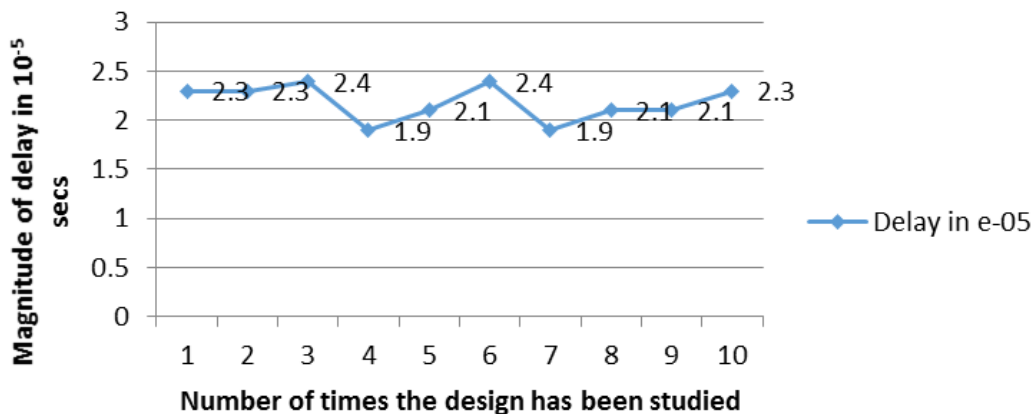

Fig 3 The Delay of Simulated Design.

where x-axis define the number of simulations done and y-axis define the magnitude of the delay elapsed (in 10^{-5} seconds) for getting the complete continuous signal at output.

The results calculated have been compared with existing performance parameters. Similar to the delay for a bit in binary flip-flop, this calculated delay has its own significance as it is the delay which appears in the design till the entire signal gets replicated at output. When variability of the design has been compared with the previous designs following results have arrived [8]. The results have been tabulated in table 2.

TABLE 2: THE VARIABILITY COMPARISONS BETWEEN VARIOUS DESIGNS.

Type of the Flip-Flop	Variability Range
TG based D flip-flop	1-2.1
TSPSC based D flip-flop	$(1-1.3)\times10^{-1}$
Low power D flip-flop	1.5-2.1
Push pull D flip-flop	2-3.1
Clocked CMOS D flip-flop	1.3-2.1
10-T based D flip-flop	1.1-1.2
Proposed Design	$\mathbf{0.8\times10^{-1}}$

V.   CONCLUSION

Memory modules form the important part of fuzzy inference and fuzzy control systems. Besides the memory, the computation speed of the circuits is of great importance. Thus, paper focused on the discussion and analysis of the D fuzzy flip-flop design. The flip-flop has been studied for the delay and variability. The design has been found to be superior to the existing designs in terms of the variation range of the delay. The design has been less sensitive to the delays in input, propagation and feedback delays. Lower variability has been observed than the existing designs except Push-pull Isolation D flip-flop. Hence, the Fuzzy D flip-flop design is more robust that is less sensitive to the variations in input and changes in the environment conditions.

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